Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.014 x .014”**

**.025”**

**.025”**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .014” X .014”**

**Backside Potential: Cathode**

**Mask Ref: CPD04**

**APPROVED BY: DK DIE SIZE .025” X .025” DATE: 10/18/21**

**MFG: CENTRAL SEMI THICKNESS .009” P/N: 1N645**

**DG 10.1.2**

#### Rev B, 7/19/02